Design of Synchronous Counters

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EECS: 1100 Digital Logic Design
The University of Toledo

Lab Assignment #11

1. Objectives

- getting familiar with *state transition* tables of synchronous counters,
- gaining experience in constructing *state transition excitation* tables of synchronous counters,
- gaining experience in using flip-flop excitation tables,
- gaining a close insight into the functioning and properties of synchronous counters,
- developing skills in the composition and testing of sequential logic circuits.

2. Prelab Assignment

2.1 THE DOWN-COUNTING BCD COUNTER

2.1.1 Data sheets of the 74LS76A dual negative edge triggered JK-flip-flop are available from the TTL Data Book.

2.1.2 Prepare a graphical representation of the state transition graph of the down-counting BCD counter with decimally encoded states, and show it as Figure 2.1.1(a). Prepare a graphical representation of the state transition graph of the down-counting BCD counter with binary encoded states, and show it as Figure 2.1.1(b).

Hint#1 In anticipation of the work to be performed under 2.1.7, provide in Figure 2.1.1(b) sufficient space to accommodate the graphical representations of unused states.

2.1.3 Designating the internal memory states in the LSB to MSB order by Q_A , Q_B , Q_C , and Q_D , prepare the state transition table of the down-counting BCD counter with binary encoded states, and show it as table T2.1-1.

2.1.4 Prepare the excitation table of the JK-flip-flop and show it as table T2.1-2.

2.1.5 Using the information from tables T2.1-1 and T2.1-2 prepare the state transition excitation table of the down-counting BCD counter with binary encoded states and show it as table T2.1-3.

Hint#2 Reduce the work for construction of T2.1-3 by making a copy of T2.1-1 and appending to it the missing columns.

Hint#3 In anticipation of the work to be performed under 2.1.7, provide in table T2.1-3 the rows for unused states, but leave the next internal state and flip-flop excitation function columns blank.

2.1.6 Using the table T2.1-3 and the Karnaugh map minimization method, derive minimized expressions of the J and K input functions of the four flip-flops in the internal state memory of the counter.

2.1.7 Check the designed counter circuit on being self-starting.

Hint#4 A counter state machine with unused states possesses the self-starting property if its state transition graph has a directed path from each unused state to some used state. [See M.Mano, Digital Design, Prentice Hall, 1991, second edition, pp.250-251 for a counter specific example, and also pp.246-247 for an example of a general state machine with unused states.]

Hint#5 A convenient way of checking if the designed counter is self-starting would be to apply the following procedure:

(a) for each unused state at a time,

- use the derived minimized expressions of the J and K input functions to determine the logical values at the inputs of the four flip-flops, and record those values into the corresponding columns of the row of the currently considered unused state;
- using the recorded input values and the characteristic table of the JK-flip-flop, determine the next states of the flip-flops, and record them into the corresponding columns of the row of the currently considered unused state;
- add to the graphical representation of the state transition graph in Figure 2.1.1(b) the directed edge which represents the derived transition from the currently considered unused state;

(b) verify that a directed path exists in the state transition graph from each unused state to a used state;

(c) if the result of the verification is positive the counter is self-starting, otherwise it is not self-starting.

State the step of the applied design procedure which should be altered if one wanted to correct a counter design which fails to verify as self-starting?

2.1.8 Prepare a computer generated drawing of the counter's logic circuit and show it as Figure 2.1.2(a).

2.1.9 Design a physical layout of the logic circuit shown in Figure 2.1-2(a). Prepare a computer generated drawing of the physical layout and show it as Figure 2.1-2(b). Provide the IC package pinouts on both drawings of Figure 2.1-2.

2.2 UP-COUNTING MODULO-6 COUNTER

2.2.1 Prepare a graphical representation of the state transition graph of the up-counting modulo-6 counter with decimally encoded states, and show it as Figure 2.2.1(a). Prepare a graphical representation of the state transition graph of the up-counting modulo-6 counter with binary encoded states, and show it as Figure 2.2.1(b).

Hint#6 In anticipation of the work to be performed under 2.2.5, provide in Figure 2.2.1(b) sufficient space to accommodate the graphical representations of unused states.

2.2.2 Prepare the state transition table of the up-counting modulo-6 counter with binary encoded states and show it as table T2.2-1. Designate the internal memory states in the LSB to MSB order by Q_A, Q_B, Q_C.

2.2.3 Using the information from tables T2.1-2 and T2.2-1 prepare the state transition excitation table of the up-counting modulo-6 counter with binary encoded states and show it as table T2.2-2.

Hint#7 Reduce the work for construction of T2.1-2 by making a copy of T2.2-1 and appending to it the missing columns.

Hint#8 In anticipation of the work to be performed under 2.2.5, provide in table T2.1-3 the rows for unused states, but leave the next internal state and flip-flop excitation function columns blank.

2.2.4 Using the table T2.1-2 and the Karnaugh map minimization method, derive minimized expressions of the J and K input functions of the four flip-flops in the internal state memory of the counter.

2.2.5 Check the designed up-counting modulo-6 counter circuit on being self-starting.

2.2.6 Prepare a computer generated drawing of the counter's logic circuit and show it as Figure 2.2.2(a).

2.2.7 Design a physical layout of the logic circuit shown in Figure 2.2-2(a). Prepare a computer generated drawing of the physical layout and show it as Figure 2.2-2(b). Provide the IC package pinouts on both drawings of Figure 2.2-2.

3. Lab Equipment and Circuit Components

3.1 EQUIPMENT

Equipment to be used includes:

- Proto boards: Power ACE, or Global PB-104, or PB-105,
- Agilent E3631A DC power supply,
- Function generator: Agilent 33120A,
- Mixed-Signal oscilloscope Agilent 54645D,
- Dell GxaEM computer system.

3.2 LOGIC GATE AND CIRCUIT COMPONENTS

- integrated circuit 7408, quod AND gates (1)
- integrated circuit 7432, quod OR gates (1)
- integrated circuit 74LS76A, dual negative-edge triggered JK-flip-flop (2)

4. Lab Assignment

4.1 EXPERIMENT WITH THE DOWN-COUNTING BCD COUNTER

4.1.1 Using as a reference the prepared physical layout drawing of Figure 2.1-2(b), build on the protoboard a physical circuit that implements the down-counting BCD counter. Figure A.4-1 shows the complete test circuit.

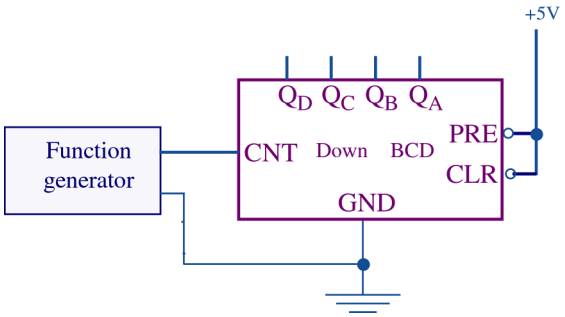

Figure A.4-1 The complete circuit for experimenting with the Down-Counting BCD Counter.

4.1.2 Connect the digital channels D0 through D4 of the Mixed-Signal oscilloscope Agilent 54645D to the circuit constructed under 4.1.1:

- digital channel D0: to the output of the function generator,
- digital channels D_1:D_4 to the outputs Q_A:Q_D of the BCD counter circuit,

Establish a ground connection. Turn on digital channels D0 through D4, and rename the channels D0 through D4 as: A, Q_A, Q_B, Q_C, Q_D respectively.

4.1.3 Adjust the frequency of the Agilent 33120A function generator to 1MHz. Set the triggering mode of the Agilent 54645D to combination 1001 on channels D1 through D4. Hit the key Single on the Agilent 54645D. Adjust the display so that the combination 1001 of the counter's output signals is positioned at the left side of the screen, and that the whole screen shows ten percent more than two periods of the signal at Q_D.

4.1.4 Save the Screen Image of the correct waveforms of channels D0 through D4 to a file named L11_414.tif on the Dell GxaEM computer system. (Alternatively, use the Screen Capture tool.)

4.1.5 Observe the captured counter's output waveforms. Compare these waveforms with the contents of Table T2.1-1.

4.2 EXPERIMENT WITH THE UP-COUNTING MODULO-6 COUNTER

4.2.1 Using as a reference the prepared physical layout drawing of Figure 2.2-1(b), build on the protoboard the test circuit shown in Figure A.4-2.

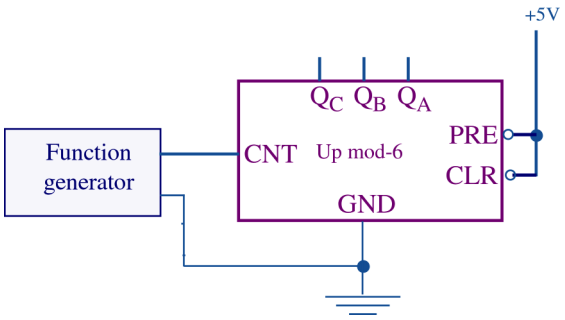

Figure A-4.2 The complete circuit for experimenting with the up-counting modulo-6 counter circuit.

4.2.2 Connect the digital channels D0 through D3 of the Mixed signal oscilloscope Agilent 54645D to the circuit shown in Figure A.4-2:

- digital channel D0: to the output of the Agilent 33120A function generator,
- digital channels D_1:D_3 to the outputs Q_A:Q_C of the up-counting modulo-6 counter circuit.

Establish a ground connection. Turn on digital channels D0 through D3, and rename the channels D0 through D3 as A, Q_A, Q_B, Q_C respectively.

4.2.3 Adjust the frequency of the Agilent 33120A function generator to 1MHz. Set the triggering mode of the Agilent 54645D to the combination 000 on channels D1 through D3. Hit the key Single on the Agilent 54645D. Adjust the display so that the combination 000 of the counter's output signals is positioned at the left side of the screen, and that the whole screen shows ten percent more than two periods of the signal at Q_C.

4.2.4 Save the Screen Image of the correct waveforms of channels D0 through D4 to a file named L11_424.tif on the Dell GxaEM computer system. (Alternatively, use the Screen Capture tool.)

4.2.5 Observe the captured counter's output waveforms. Compare these waveforms with the contents of Table T2.2-1.

5. Lab Report

To be considered complete, the lab report must contain the following,

1. Cover sheet - Lab style, filled out,
2. The state transition and state transition excitation tables prepared under 2.1 through 2.2.
3. The Karnaugh maps and minimized expressions of J and K input functions derived under 2.1 and 2.2.
4. The logic and physical circuit diagrams prepared under 2.1 through 2.2.
5. The waveforms captured in experiments 4.1 through 4.2.
6. Answers to all questions asked in conjunction with experiments 4.1 through 4.2.
7. A report on items not already included under 1. through 6. above, which includes:
   - a discussion of the insights gained through the conducted experiments,
   - textual description and graphical/ tabular illustration of the design procedure(s),
   - description of implemented testing procedures,
   - conclusions reached as a result of performing the lab experiment,
   - comments and suggestions that might lead to easier and/or deeper understanding of the topics covered by the assignment.